WHAT IS CLAIMED IS:

1. A memory system comprising:

a plurality of storage cells that each store a data value; and

a memory control system that identifies particular ones of said storage cells as targets of read and write commands;

wherein data values written to ones of said plurality of storage cells identified by said memory control system identify tasks to be performed later;

wherein said memory control system determines an order of performing said tasks by controlling an order of reading data values from said plurality of storage cells;

wherein said memory control system reads out said data values so that a selected task is performed n times if and only if all other ones of said tasks have been performed n-1 times; and

wherein said memory control system allocates only one storage cell per task even if tasks are performed repeatedly.

2. The memory system of claim 1 wherein said memory control system overwrites an oldest previously stored data value with a new data value.

3. The memory system of claim 1 wherein said memory control system comprises:

a write pointer that identifies a next storage cell to be written to; and

a plurality of read pointers identifying a next storage cell to be read from, each of said plurality of read pointers associated with one of a plurality of priority levels.

4. The memory system of claim 3 wherein said memory control system further comprises:

a plurality of registers, each of said registers identifying a number of storage cells implementing a particular list associated with one of said plurality of priority levels; .

5. The memory system of claim 4 wherein one of said plurality of registers associated with a highest priority lists increments after each write operation.

6. The memory system of claim 5 wherein said memory control system selects a particular storage cell for reading based on a value of a particular read pointer associated with a particular priority level.

7. The memory system of claim 6 wherein said memory control system changes said current priority level to a next lower priority level when said register associated with said current priority level is zero and said register associated with said next lower priority level has a value greater than zero.

8. The memory system of claim 6 wherein a register associated with a priority level one lower than a current priority level is decremented after a write operation that overwrites a value that has been read out using said read pointer associated with said current priority level.

9. The memory system of claim 8 wherein said register associated with said priority level one lower than said current priority level decrements below zero.

10. The memory system of claim 3 wherein said plurality of storage cells are each identified by a location in a circular address space and said write pointer and said read pointers store addresses in said address space.

11. The memory system of claim 1 wherein said tasks comprise retransmissions of data in a communication system.

12. The memory system of claim 1 wherein said tasks comprise requests for retransmission of data in a communication system.

13. A memory system comprising:

a plurality of storage cells that each store a data value; and

a memory control system that identifies particular ones of said storage cells as targets of read and write commands;

wherein said memory control system determines an order of reading data values from said plurality of storage cells;

wherein said memory control system reads out said data values so that a data value is read out n times if and only if all other ones of said data values have been read out n-1 times; and

wherein said memory control system allocates only one storage cell per data value.

14. A method for operating a memory device including a plurality of storage cells:

dynamically partitioning said memory device into a plurality of priority lists;

directing new data to be stored in said memory device to storage cells belonging to a highest priority list of said plurality of priority lists;

reading data from said memory device only from a highest priority non-empty priority list; and

transferring data read in said reading step to a next lower priority list after reading without moving data between storage cells.

15. The method of claim 14 wherein dynamically partitioning comprises:

providing a write pointer and a plurality of read pointers each of said read pointers corresponding to one of a plurality of priority levels.

16. The method of claim 15 wherein directing comprises:

writing data to a location in said memory device determined by said write pointer and thereafter incrementing said write pointer.

17. The method of claim 15 wherein reading comprises:

reading data from a location in said memory device determined by one of said plurality of read pointers corresponding to said highest priority non-empty priority list.

18. The method of claim 17 wherein dynamically partitioning further comprises:

providing for each of said priority lists a count register indicating an allocated number of storage cells.

19. The method of claim 18 wherein transferring comprises:

incrementing said read pointer corresponding to said highest priority non-empty priority list;

decrementing one of said count registers corresponding to said highest priority non-empty priority list; and

incrementing one of said count registers corresponding to a next highest priority priority list.

20. The method of claim 14 wherein said count register corresponding to said next highest priority priority list is incremented only after a delay.

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